



# Pentium Pro™ and SDRAM Frequency Generator

## General Description

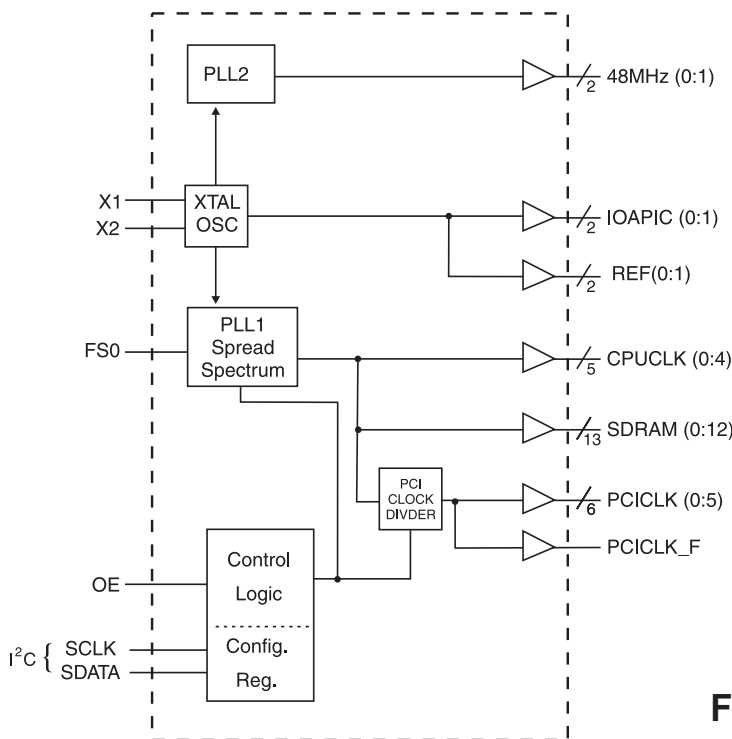
The ICS9150-02 generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel Pentium Pro. Two different reference frequency multiplying factors are externally selectable with smooth frequency transitions. An output enable is provided for testability.

High drive PCICLK & SDRAM outputs typically provide greater than 1V/ns slew rate into 30 pF loads. CPUCLK outputs typically provide better than 1V/ns slew rate into 20 pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates.

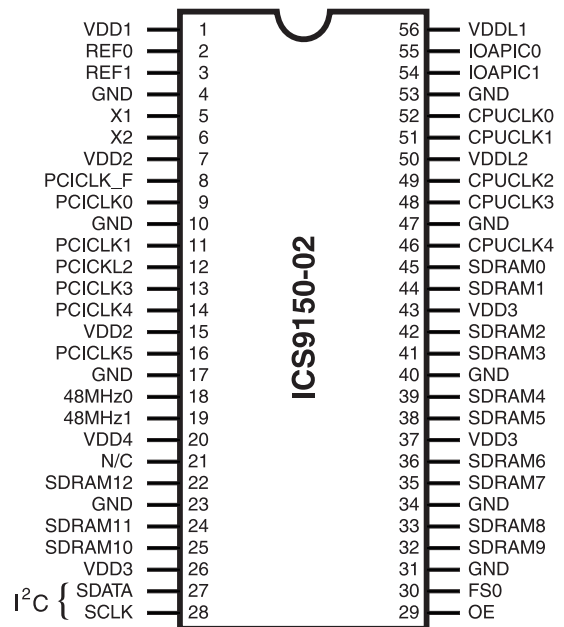
## Features

- Generates five processor, six bus, two 14.31818MHz and 13 SDRAM clocks.
- Synchronous clocks skew matched to 250 ps window on PCLKs and 500 ps window on BCLKs
- Test clock mode eases system design
- Spread Spectrum available
- I<sup>2</sup>C interface for programming
- Skew from CPU (earlier) to PCI clock -1 to 4ns, center 2.6ns
- 3.0V – 3.7V supply range
- 56-pin SSOP package

## Block Diagram



## Pin Configuration



**56-Pin SSOP**

## Functionality

FS0	CPUCLK, SDRAM (MHz)	X1, REF (MHz)	PCICLK (MHz)
0	60.0	14.318	30
1	66.6	14.318	33.3

Pentium is a trademark of Intel Corporation



### Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2, 3	REF (0:1)	OUT	14.318 MHz reference clock outputs.
4, 10, 17, 23, 31, 34, 40, 47, 53	GND	PWR	Ground.
5	X1	IN	14.318MHz input. Has internal load cap,(33pF).
6	X2	OUT	Crystal output. Has internal load cap (33pF) and feedback resistor to X1
8	PCICLK_F	OUT	Free running BUS clock.
9, 11, 12, 13, 14, 16	PCICLK (0:5)	OUT	BUS clock outputs.
18, 19	48MHz	OUT	48MHz clock outputs
21	N/C	-	Pins are not internally connected.
27	SDATA	IN	Serial data in for serial config port.
28	SCLK	IN	Clock input for serial config port.
29	OE	IN	Logic input for output enable, tristates all outputs when low.
30	SEL 66/60#	IN	Selects 60MHz or 66MHz for SDRAM and CPU.
1, 7, 15, 20, 26, 37, 43	VDD2, VDD1, VDD3, VDD4	PWR	Nominal 3.3V power supply. See power groups for function.
50, 56	VDDL2, VDDL1	PWR	CPU and IOAPIC clock buffer power supply (2.5 - VDD)
22, 24, 25, 32, 33, 35, 36, 38, 39, 41, 42, 44, 45	SDRAM (0:12)	OUT	SDRAM clocks (60/66.6MHz)
54, 55	IOAPIC (1:0)	OUT	IOAPIC clock output. (14.31818 MHz) Powered by VDDL1
46, 48, 49, 51, 52	CPUCLK (0:4)	OUT	CPU Output clocks. Powered by VDDL2 (60 or 66.6MHz)

### Power Groups

VDD1 = REF (0:1), X1, X2  
 VDD2 = PCICLK\_F, PCICLK (0:5)  
 VDD3 = SDRAM(0:12), Supply for PLL core  
 VDD4 = 48 MHz  
 VDDL1 = IOAPIC (0:1)  
 VDDL2 = CPUCLK (0:4)



## Technical Pin Function Descriptions

### **VDD(1,2,3,4)**

This is the power supply to the internal core logic of the device as well as the clock output buffers for REF(0:1), PCICLK, 48MHz (0:1) and SDRAM(0:7).

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

### **VDDL1,2**

This is the power supplies for the CPUCLK and IOAPCI output buffers. The voltage level for these outputs may be 2.5 or 3.3volts. Clocks from the buffers that each supplies will have a voltage swing from Ground to this level. For the actual Guaranteed high and low voltage levels of these Clocks, please consult the DC parameter table in this Data Sheet.

### **GND**

This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

### **X1**

This input pin serves one of two functions. When the device is used with a Crystal, X1 acts as the input pin for the reference signal that comes from the discrete crystal. When the device is driven by an external clock signal, X1 is the device input pin for that reference clock. This pin also implements an internal Crystal loading capacitor that is connected to ground. With a nominal value of 33pF no external load cap is needed for a  $C_L=17$  to 18pF crystal.

### **X2**

This Output pin is used only when the device uses a Crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the discrete Crystal. The X2 pin will also implement an internal Crystal loading capacitor nominally 33pF.

### **CPUCLK (0:4)**

These Output pins are the Clock Outputs that drive processor and other CPU related circuitry that requires clocks which are in tight skew tolerance with the CPU clock. The voltage swing of these Clocks are controlled by the Voltage level applied to the VDDL2 pin of the device. See the Functionality Table for a list of the specific frequencies that are available for these Clocks and the selection codes to produce them.

### **SDRAM(0:12)**

These Output Clocks are use to drive Dynamic RAM's and are low skew copies of the CPU Clocks. The voltage swing of the SDRAM's output is controlled by the supply voltage that is applied to VDD3 of the device, operates at 3.3 volts.

### **IOAPIC (0:1)**

These Outputs are fixed frequency Output Clocks that run at the Reference Input (typically 14.31818MHz) . Its voltage level swing is controlled by VDDL1 and may operate at 2.5 or 3.3volts.

### **REF (0:1)**

The REF Output is a fixed frequency Clock that runs at the same frequency as the Input Reference Clock X1 or the Crystal (typically 14.31818MHz) attached across X1 and X2.

### **PCICLK\_F**

This Output is equal to PCICLK(0:5).

### **PCICLK (0:5)**

These Output Clocks generate all the PCI timing requirements for a Pentium/Pro based system. They conform to the current PCI specification. They run at 1/2 CPU frequency.

### **FS0**

This Input pin controls the frequency of the Clocks at the CPU, PCICLK and SDRAM output pins. If a logic "1" value is present on this pin, the 66.6 MHz Clock will be selected. If a logic "0" is used, the 60MHz frequency will be selected.

### **I<sup>2</sup>C**

The SDATA and SCLOCK Inputs are use to program the device. The clock generator is a slave-receiver device in the I<sup>2</sup>C protocol. It will allow read-back of the registers. See configuration map for register functions. The I<sup>2</sup>C specification in Philips I<sup>2</sup>C Peripherals Data Handbook (1996) should be followed.

### **48MHz**

This is a fixed frequency clock that is typically used to drive Super I/O peripheral device needs and USB.

### **OE**

Output Enable tristates the outputs when held low. This pin will override the I<sup>2</sup>C Byte 0 function, so that the outputs will be tristated when the OE is low regardless of the I<sup>2</sup>C defined function. When OE is high, the I<sup>2</sup>C function is in active control.



### General I<sup>2</sup>C serial interface information

- A. For the clock generator to be addressed by an I<sup>2</sup>C controller, the following address must be sent as a start sequence, with an acknowledge bit between each byte.

Clock Generator Address (7 bits)	ACK	+ 8 bits dummy command code	ACK	+ 8 bits dummy Byte count	ACK
A(6:0) & R/W#					
D2(H)					

Then Byte 0, 1, 2, etc in sequence until STOP.

- B. The clock generator is a slave/receiver I<sup>2</sup>C component. It can "read back "(in Philips I<sup>2</sup>C protocol) the data stored in the latches for verification. (set R/W# to 1 above). There is no BYTE count supported, so it does not meet the Intel SMB PIIX4 protocol.

Clock Generator Address (7 bits)	ACK	Byte 0	ACK	Byte 1	ACK
A(6:0) & R/W#					
D3(H)					

Byte 0, 1, 2, etc in sequence until STOP.

- C. The data transfer rate supported by this clock generator is 100K bits/sec (standard mode)
- D. The input is operating at 3.3V logic levels.
- E. The data byte format is 8 bit bytes.
- F. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
- G. In the power down mode (PWR\_DWN# Low), the SDATA and SCLK pins are tristated and the internal data latches maintain all prior programming information.
- H. At power-on, all registers are set to a default condition. See Byte 0 detail for default condition, Bytes 1 through 5 default to a 1 (Enabled output state)

### Serial Configuration Command Bitmaps

Byte 0: Functional and Frequency Select Clock Register (default = 0)

BIT	PIN#	DESCRIPTION	PWD
Bit 7	-	Reserved	0
Bit 6	-	Must be 0 for normal operation	0
Bit 5	-	Must be 0 for normal operation	0
		In Spread Spectrum, Controls type (0=centered, 1=down spread)	0
Bit 4	-	Must be 0 for normal operation	0
		In Spread Spectrum, Controls Controls Spreading %(0=1.5%, 1=0.5%)	0
Bit 3	-	Reserved	0
Bit 2	-	Reserved	0
Bit 1	-	Bit1	0
Bit 0		Bit0	
		1 - Tri-State	
		0 - Spread Spectrum Enable	
		0 - 1 - Testmode	0
		0 - 0 - Normal operation	0

Note: PWD = Power-Up Default

I<sup>2</sup>C is a trademark of Philips Corporation



Select Functions

FUNCTION DESCRIPTION	OUTPUTS				
	CPU	PCI, PCL_F	SDRAM	REF	IOAPIC
Tri - State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	TCLK/2 <sup>1</sup>	TCLK/4 <sup>1</sup>	TCLK/2 <sup>1</sup>	TCLK <sup>1</sup>	TCLK <sup>1</sup>

Notes:

1. REF is a test clock on the X1 inputs during test mode.

Byte 1: CPU Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	46	1	CPUCLK4 (Act/Inact)
Bit 3	48	1	CPUCLK3 (Act/Inact)
Bit 2	49	1	CPUCLK2 (Act/Inact)
Bit 1	51	1	CPUCLK1 (Act/Inact)
Bit 0	52	1	CPUCLK0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 3: SDRAM Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	35	1	SDRAM7 (Act/Inact)
Bit 6	36	1	SDRAM6 (Act/Inact)
Bit 5	38	1	SDRAM5 (Act/Inact)
Bit 4	39	1	SDRAM4 (Act/Inact)
Bit 3	41	1	SDRAM3 (Act/Inact)
Bit 2	42	1	SDRAM2 (Act/Inact)
Bit 1	44	1	SDRAM1 (Act/Inact)
Bit 0	45	1	SDRAM0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 5: Peripheral Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	2	1	REF0 (Act/Inact)
Bit 5	54	1	IOAPIC1 (Act/Inact)
Bit 4	55	1	IOAPIC0 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	3	1	REF1 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 2: PCICLK Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	8	1	PCICLK_F (Act/Inact)
Bit 5	16	1	PCICLK5 (Act/Inact)
Bit 4	14	1	PCICLK4 (Act/Inact)
Bit 3	13	1	PCICLK3 (Act/Inact)
Bit 2	12	1	PCICLK2 (Act/Inact)
Bit 1	11	1	PCICLK1 (Act/Inact)
Bit 0	9	1	PCICLK0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 4: SDRAM Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	18	1	48 MHz0 (Act/Inact)
Bit 6	19	1	48 MHz1 (Act/Inact)
Bit 5	-	1	Reserved
Bit 4	22	1	SDRAM12 (Act/Inact)
Bit 3	24	1	SDRAM11 (Act/Inact)
Bit 2	25	1	SDRAM10 (Act/Inact)
Bit 1	32	1	SDRAM9 (Act/Inact)
Bit 0	33	1	SDRAM8 (Act/Inact)

Byte 6: Peripheral Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Notes:

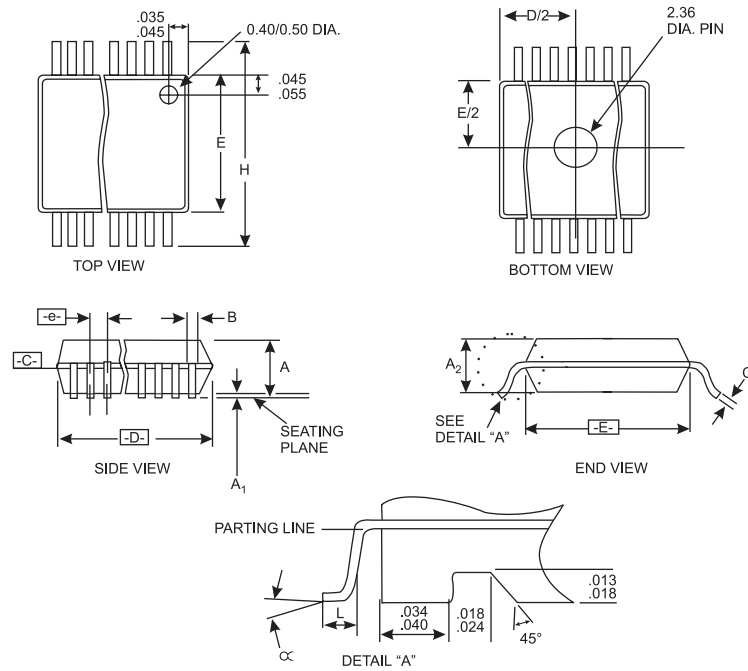
1. Byte 6 is reserved by Integrated Circuit Systems for future applications.





# ICS9150-02

## Preliminary Product Preview



### SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016	AD	.720	.725	.730	56
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∞	0°	5°	8°					
X	.085	.093	.100					

### Ordering Information

#### ICS9150F-02

Example:

**ICS XXXX F - PPP**

